AMENDMENTS TO THE CLAIMS:

1-19. (Cancelled)

20. (Currently Amended) An integrating apparatus comprising:

a plurality of integrating circuits each operable to integrate an input signal and to output an integrated signal, said plurality of integrating circuits each having a different fall time constant;

an output unit operable to selectively derive an output having a lowest level from among integrated signals output from said plurality of integrating circuits; and

a plurality of first amplifiers operable to amplify the input signal and to output the amplified input signal to said plurality of integrating circuits, respectively; wherein each of said plurality of first amplifiers has an amplification factor corresponding to the fall time constant of a respective one of said plurality of integrating circuits to which the input signal is inputted such that the amplification factor is larger when the fall time constant is smaller; and

wherein each of said plurality of integrating circuits comprises:

an adder operable to add the amplified input signal and a feedback signal, and to output a resultant added signal;

a delaying unit operable to delay the resultant added signal and to produce a delayed output signal; and

a second amplifier operable to amplify the delayed output signal and to produce an amplified output signal~~, and~~

wherein the amplified output signal output from said second amplifier is inputted to said adder as the feedback signal, and the resultant added signal is produced as the integrated signal output from said integrating circuit.

21. (Previously Presented) The integrating apparatus according to claim 20, wherein said plurality of integrating circuits are each controlled so that an average value of the output level becomes higher as the fall time constant becomes smaller.

22. (Cancelled)

23. (Cancelled)

24. (Previously Presented) The integrating apparatus according to claim 20, wherein said second amplifier has a gain of less than one.

25. (Previously Presented) The integrating apparatus according to claim 24, wherein said adder is operable to sample and compute the integrated signal at predetermined sampling time intervals.

26. (Previously Presented) The integrating apparatus according to claim 25, wherein said delaying unit is operable to delay the integrated signal on a timescale of the predetermined sampling time intervals.

27. (Previously Presented) The integrating apparatus according to claim 20, wherein said adder is operable to sample and compute the integrated signal at predetermined sampling time intervals.

28. (Previously Presented) The integrating apparatus according to claim 27, wherein said delaying unit is operable to delay the integrated signal on a timescale of the predetermined sampling time intervals.

29. (Currently Amended) An audio system comprising:

a detecting unit operable to detect a noise signal in response to a noise level;

a plurality of integrating circuits each operable to integrate the noise signal detected by said detecting unit and to output an integrated signal, said plurality of integrating circuits each having a different fall time constant;

an output unit operable to selectively derive an output signal having a lowest level from among integrated signals output from said plurality of integrating circuits, and to output a control signal as the selectively derived output signal;

an audio source operable to output an audio signal;

an attenuating unit operable to attenuate the audio signal in response to a level of the control signal outputted by said output unit; and

a plurality of first amplifiers operable to amplify the ~~input~~ noise signal and to output the amplified ~~input~~ noise signal to said plurality of integrating circuits, respectively; wherein each of said plurality of first amplifiers has an amplification factor corresponding to the fall time constant of a respective one of said plurality of integrating circuits to which the ~~input~~ noise signal is inputted such that the amplification factor is larger when the fall time constant is smaller; and

wherein each of said plurality of integrating circuits comprises:

an adder operable to add the amplified ~~input~~ noise signal and a feedback signal, and to output a resultant added signal;

a delaying unit operable to delay the resultant added signal and to produce a delayed output signal; and

a second amplifier operable to amplify the delayed output signal and to produce an amplified output signal,~~; and~~

wherein the amplified output signal output from said second amplifier is inputted to said adder as the feedback signal, and the resultant added signal is produced as the integrated signal output from said integrating circuit.

30. (Previously Presented) The audio system according to claim 29, wherein said plurality of integrating circuits are each controlled so that an average value of the output level becomes higher as the fall time constant becomes smaller.

31. (Cancelled)

32. (Cancelled)

33. (Currently Amended) A signal processing apparatus comprising:

at least one sensor operable to detect a level of a physical value or a chemical value; and

[[,]] an integrating apparatus to which an output of said at least one sensor is supplied, said integrating apparatus comprising:

a plurality of integrating circuits each operable to integrate an input signal and to output an integrated signal, said plurality of integrating circuits each having a different fall time constant;

an output unit operable to selectively derive an output having a lowest level from among integrated signals output from said plurality of integrating circuits; and

a plurality of first amplifiers operable to amplify the input signal and to output the amplified input signal to said plurality of integrating circuits, respectively;

wherein each of said plurality of first amplifiers has an amplification factor corresponding to the fall time constant of a respective one of said plurality of integrating circuits to which the input signal is inputted such that the amplification factor is larger when the fall time constant is smaller; and

wherein each of said plurality of integrating circuits comprises

an adder operable to add the amplified input signal ~~arid~~ and a feedback signal, and to output a resultant added signal,

a delaying unit operable to delay the resultant added signal and to produce a delayed output signal, and

a second amplifier operable to amplify the delayed output signal and to produce ~~ate~~ an amplified output signal,

wherein the amplified output signal output from said second amplifier is inputted to said ~~added~~ adder as the feedback signal, and the resultant added signal is produced as the integrated signal output from said integrating circuit.

34. (Currently Amended) The signal processing apparatus according to claim 33, wherein said plurality of integrating circuits are each controlled so that an average value of the output levels becomes higher as the fall time constant becomes smaller.

~~sensor is supplied.~~

35. (Cancelled)

36. (Cancelled)

37. (Currently Amended) The signal processing apparatus according to claim 33, wherein said second amplifier has a gain of less than one.

~~sensor is supplied.~~

38. (Currently Amended) The signal processing apparatus according to claim 37, wherein said adder is operable to sample and compute the integrated signal at predetermined sampling intervals.

~~sensor is supplied.~~

39. (Currently Amended) The signal processing apparatus according to claim 38, wherein said delaying unit is operable to delay the integrated signal on a timescale of the predetermined sampling time intervals.

~~sensor is supplied.~~

40. (Currently Amended) The signal processing apparatus according to claim 33, wherein said adder is operable to sample and compute the integrated signal at predetermined sampling time intervals.

~~sensor is supplied.~~

41. (Currently Amended) ~~A~~ The signal processing apparatus ~~comprising:~~ according to claim 40, wherein said delaying unit is operable to delay the integrated signal on a timescale of the predetermined sampling time intervals.

~~at least one sensor operable to detect a level of a physical value or a chemical value; and~~

~~said integrating apparatus according to claim 28, to which an output of said at least one sensor is supplied.~~